REMARKS

Applicants appreciate the Examiner's thorough consideration provided the present application. Claims 1, 2, 4-8, 10 and 12-14 are now present in the application. Claims 1, 2, 4, 8 and 10 have been amended. Claims 3, 9 and 11 have been cancelled. Claims 1 and 8 are independent. Reconsideration of this application, as amended, is respectfully requested.

Claim Rejections Under 35 U.S.C. §112

Claims 3 and 10 [sic., 3 and 11] stand rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. This rejection is respectfully traversed.

As the Examiner will note, claims 3 and 10 have been cancelled. Therefore, this rejection has been obviated and/or rendered moot. Reconsideration and withdrawal of the rejection under 35 U.S.C. § 112, first paragraph, are therefore respectfully requested.

Claim Rejections Under 35 U.S.C. § 103

Claims 1-14 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicants' Admitted Prior Art (AAPA in view of Utsumi, U.S. Patent No. 6,983,281. This rejection is respectfully traversed.

In light of the foregoing amendments to the claims, Applicants respectfully submit that this rejection has been obviated and/or rendered moot. As the Examiner will note, independent claims 1 and 8 have been amended.

Independent claim 1 now recites "providing the IO card with a socket therein; inserting the memory card entirely into the socket of the IO card; connecting the IO card to the host

system; and generating a bus control signal through an IO controller on the IO card to switch to a first data bus or a second data bus located in the IO card thereby to change data transmitting path between the memory card and the host system."

Independent claim 8 now recites "providing the IC card with a first data bus and a second data bus, the first data bus and the second data bus being directly connected to the host system; providing a switch to selectively directly connect the inserted memory card to one of the first and second data bus; and generating a bus control signal through an IO controller located in the IO card, thereby controlling the switch to selectively directly connect the inserted memory card to one of the first and second data bus."

Support for the above combinations of steps can be found in FIGs. 3-5 as originally filed. Applicants respectfully submit that the above combinations of steps as set forth in amended independent claims 1 and 8 are not disclosed nor suggested by the references relied on by the Examiner.

Claim 1

AAPA in FIG. 2 discloses that the IO card 203 is inserted into a slot of a memory 202. However, AAPA in FIG. 2 fails to disclose that the IO card 203 has a socket and that the memory card 202 is entirely inserted into the socket of the IO card 203. Therefore, AAPA fails to teach "providing the IO card with a socket therein" and "inserting the memory card entirely into the socket of the IO card" as recited in amended claim 1.

Utsumi also fails to cure the deficiencies of AAPA. In particular, Utsumi nowhere discloses how to insert the memory card 40A/B into the recorder 1, and therefore fails to teach

"providing the IO card with a socket therein" and "inserting the memory card entirely into the socket of the IO card" as recited in amended claim 1.

Claim 8

The Examiner has correctly acknowledged that AAPA fails to teach generating a bus control signal to switch the connection between the memory card and one of the first and second data buses of the IO card. In fact, AAPA nowhere discloses two data buses of the IO card. Therefore, AAPA fails to teach "providing the IC card with a first data bus and a second data bus, the first data bus and the second data bus being directly connected to the host system; providing a switch to selectively directly connect the inserted memory card to one of the first and second data bus; and generating a bus control signal through an IO controller located in the IO card, thereby controlling the switch to selectively directly connect the inserted memory card to one of the first and second data bus."

Utsumi in FIG. 4 discloses that a switch 3d of a security block 3 is operated to feed the data from the CPU2 to either the ATRAC3 decoder 83 or the ADPCM decoder 79. After the data is decoded, the decoded data is sent to an external audio output device (seemed to be referred by the Examiner as the host system). However, Utsumi fails to teach "the first data bus and the second data bus being directly connected to the host system" as recited in amended claim 8 because the data from the CPU 2 is not directly sent to the external audio output device. Instead, the data have to be decoded by the ATRAC3 decoder 83 or the ADPCM decoder 79 before being sent to the external audio output device.

In addition, Utsumi's memory card 40A/B is simply connected to the CPU 2 via a single data bus, and the switch 3d is located between the CPU2 and the ATRAC3 decoder 83 or the ADPCM decoder 79. Therefore, Utsumi also fails to teach "providing a switch to selectively directly connect the inserted memory card to one of the first and second data bus" as recited in amended claim 8.

Accordingly, neither of the references utilized by the Examiner individually or in combination teaches or suggests the limitations of amended independent claims 1 and 8 or their dependent claims. Therefore, Applicants respectfully submit that all of the claims clearly define over the teachings of the references relied on by the Examiner.

Accordingly, reconsideration and withdrawal of the rejections under 35 U.S.C. § 103 are respectfully requested.

CONCLUSION

Since the remaining patents cited by the Examiner have not been utilized to reject the claims, but merely to show the state of the prior art, no further comments are necessary with respect thereto.

It is believed that a full and complete response has been made to the Office Action, and that as such, the Examiner is respectfully requested to send the application to Issue.

In the event there are any matters remaining in this application, the Examiner is invited to contact Joe McKinney Muncy, Registration No. 32,334 at (703) 205-8000 in the Washington, D.C. area.

Pursuant to 37 C.F.R. §§ 1.17 and 1.136(a), Applicants respectfully petition for a two (2) month extension of time for filing a response in connection with the present application and the required fee is attached herewith.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§1.16 or 1.17; particularly, extension of time fees.

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Respectfully submitted,

By _____
Joe McKinney Muncy
Registration No.: 32,334 #28580
BIRCH, STEWART, KOLASCH & BIRCH, LLP
8110 Gatehouse Road
Suite 100 East
P.O. Box 747
Falls Church, Virginia 22040-0747
(703) 205-8000
Attorney for Applicant